# P-Channel 20-V (D-S) MOSFET

## CHARACTERISTICS

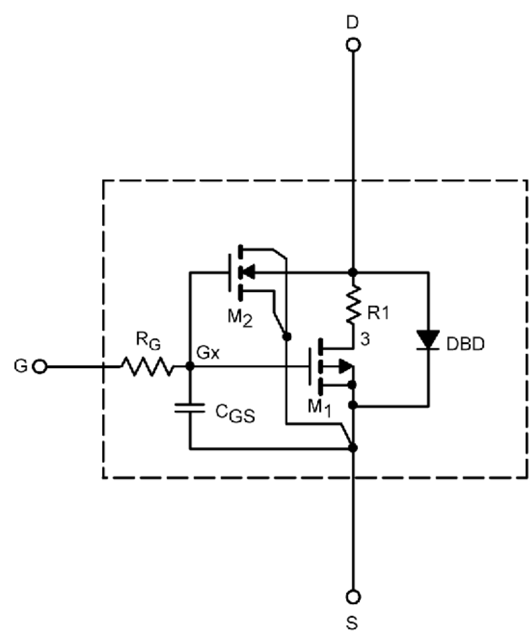
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

## DESCRIPTION

The attached spice model describes the typical electrical characteristics of the P-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## SUBCIRCUIT MODEL SCHEMATIC

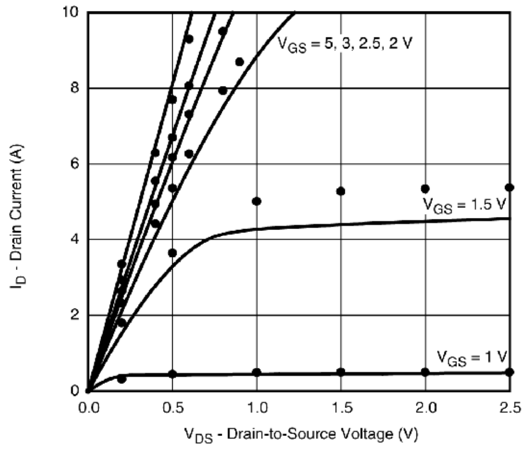


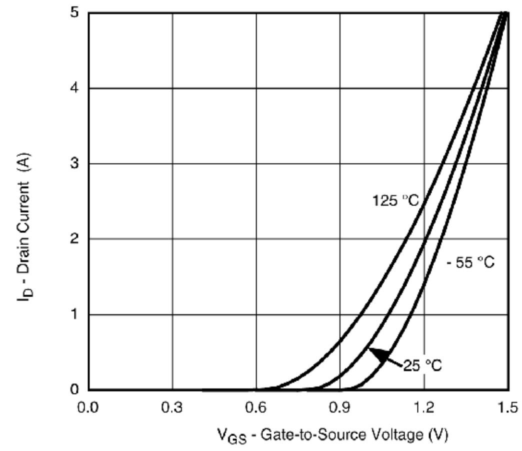

This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

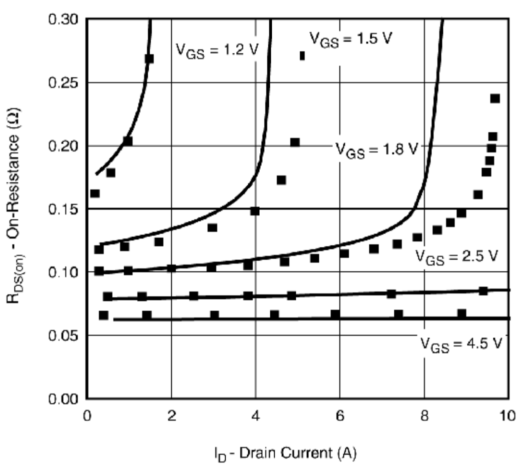
| SPECIFICATIONS ($T_J$ = 25 °C UNLESS OTHERWISE NOTED) | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Condition** | **Simulated Data** | **Measured Data** | **Unit** |
| **Static** | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = - 250 µA | 0.68 | | V |
| Drain-Source On-State Resistance[a] | $Rr_{DS(on)}$ | $V_{GS}$ = - 4.5 V, $I_D$ = - 1 A | 0.063 | 0.070 | Ω |
| | | $V_{GS}$ = - 2.5 V, $I_D$ = - 1 A | 0.079 | 0.082 | |
| | | $V_{GS}$ = - 1.8 V, $I_D$ = - 1 A | 0.101 | 0.097 | |
| | | $V_{GS}$ = - 1.5 V, $I_D$ = - 0.70 A | 0.124 | 0.115 | |
| | | $V_{GS}$ = - 1.2 V, $I_D$ = - 0.20 A | 0.177 | 0.165 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = - 10 V, $I_D$ = - 1 A | 6.4 | 6.5 | S |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = - 1 A | - 0.73 | - 0.70 | V |
| **Dynamic[b]** | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = - 10 V, $V_{GS}$ = 0 V, f = 1 MHz | 679 | 700 | pF |
| Output Capacitance | $C_{oss}$ | | 128 | 130 | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 78 | 80 | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = - 10 V, $V_{GS}$ = - 5 V, $I_D$ = - 1 A | 7.3 | 10.5 | nC |
| | | $V_{DS}$ = - 10 V, $V_{GS}$ = - 4.5 V, $I_D$ = - 1 A | 6.6 | 9.5 | |
| Gate-Source Charge | $Q_{gs}$ | | 0.90 | 0.90 | |
| Gate-Drain Charge | $Q_{gd}$ | | 2.2 | 2.2 | |

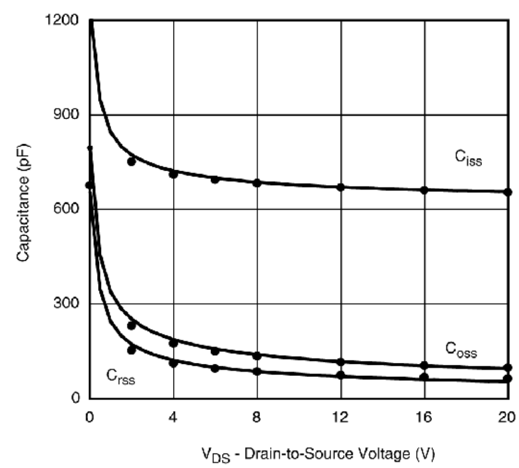
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

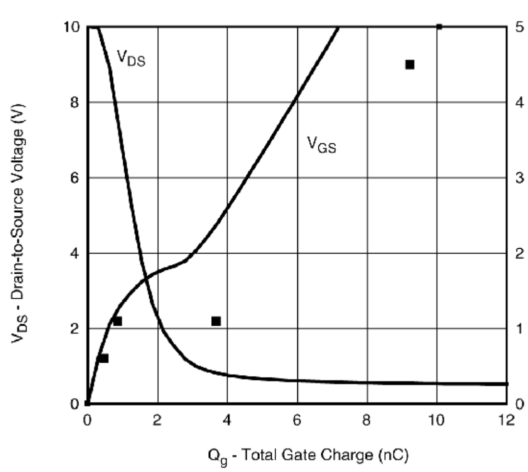
COMPARISON OF MODEL WITH MEASURED DATA ($T_J$ = 25 °C UNLESS OTHERWISE NOTED)

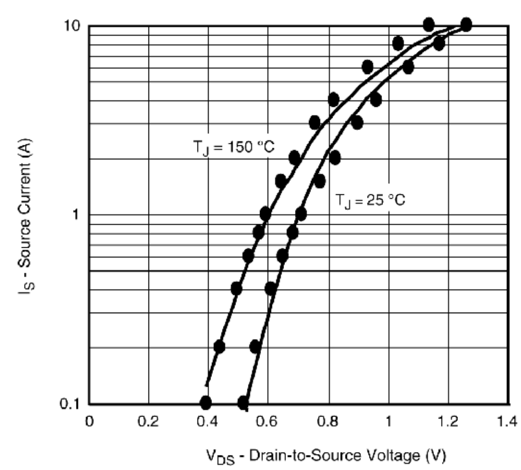



Note: Dots and squares represent measured data.

# Disclaimer

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